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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,422	03/18/2004	Min Gyu Lim	TJK/454	5542

27717 7590 03/30/2005

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EXAMINER	
ORTIZ, EDGARDO	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,422	LIM, MIN GYU	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because in Figure 4 the substrate is identified by the number 100, however the correct number should be 200 so that it is consistent with Applicant's disclosure, which specifically identifies the substrate as 200. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-6, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art as disclosed in figures 1-3C and their description on pages 1-7 of the instant application in view of Kanamori (U.S. Patent No. 6,414,346). With regard to Claim 4, Applicant's admitted prior art discloses a method for fabricating a mask ROM comprising the steps of:

providing (figure 1) a substrate (100) where a memory cell array region (I) and a segment select region (II) are defined;

forming an element isolation film and an isolating pattern at the outer portion of the memory cell array region (page 1, lines 23-25 and page 2, line 1 of the instant application);

forming (figure 1) a plurality of buried layers (110) aligned over the resultant structure in a first direction by a predetermined interval (page 2, lines 1-3 of the instant application), and surrounded by the isolating pattern; and

forming (figure 1) a plurality of gates (114) aligned in a second direction to cross the buried layers in an orthogonal direction (page 2, lines 3-5 of the instant application).

Applicant's admitted prior art fails to disclose the claimed step of providing an element isolating film and isolating pattern in the outer portion of the segment select region. However, Kanamori discloses (figure 5) a mask ROM device (column 12, lines 26-29) which, includes a memory cell array region (region 2), a peripheral circuit region (region 3) and element separation insulation films (9) which are formed in an outer portion of the peripheral circuit region, as can be seen

from the top and bottom portions of figure 5, wherein the element separation insulation films (9) are formed on outer edges of the peripheral circuit region.

Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the method as disclosed by Applicant's admitted prior art to include the claimed step of providing an element isolating film and isolating pattern in the outer portion of the segment select region, as suggested by Kanamori, in order to allow separation of elements in the segment select region by using an ordinary method such as trench insulation separation, thereby readily manufacturing an element isolating film even in the case of a complex form (column 4, lines 59-65).

With regard to Claim 5, Applicant's admitted prior art discloses (figure 3A) forming a trench at the outer portion of the memory cell array region (page 4, lines 19-21), forming an insulating layer on the substrate having the trench (page 4, lines 21-22) and etching the insulating layer (page 4, lines 23-25 of the instant application).

Applicant's admitted prior art fails to disclose the claimed step of forming a trench at the outer portion of the segment select region. However, Kanamori discloses (figure 5) a mask ROM device (column 12, lines 26-29) which, includes a memory cell array region (region 2), a peripheral circuit region (region 3) and element separation insulation films (9) which are formed in an outer portion of the peripheral circuit region, as can be seen from the top and bottom

portions of figure 5, wherein the element separation insulation films (9) are formed on outer edges of the peripheral circuit region (2).

Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the method as disclosed by Applicant's admitted prior art to include the claimed step of forming a trench at the outer portion of the segment select region, as suggested by Kanamori, in order to allow separation of elements in the segment select region by using an ordinary method such as trench insulation separation, thereby readily manufacturing an element isolating film even in the case of a complex form (column 4, lines 59-65).

With regard to Claim 6, Applicant's admitted prior art discloses that the insulating layer is etched according to an etch-back process or a chemical-mechanical process (page 4, lines 21-25 of the instant application).

With regard to Claim 8, a further difference between the claimed invention and Applicant's admitted prior art is, the claimed depth of the trenches. However, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the method as disclosed by Applicant's admitted prior art to include the claimed trench-depth, in order to enhance the isolation between the active and peripheral regions of the substrate.

With regard to Claim 9, Applicant's admitted prior art discloses (figure 3c) the steps of:

forming a protective film (120) on the substrate (100) having the gates (114);

forming a contact (122) to partially expose the buried layer of the segment select region (II), by etching the protective film (page 5, lines 18-22); and

forming a bit-line to cover the contact (page 5, lines 18-22 of the instant application).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art as disclosed in figures 1-3C and their description on pages 1-7 of the instant application in view of Kanamori (U.S. Patent No. 6,414,346) and further in view of Wu (U.S. Patent No. 6,057,195). With regard to Claim 7, Applicant's admitted prior art and Kanamori essentially disclose the claimed invention but fail to show, the claimed steps of forming the buried layers. However, Wu discloses (figures 4 and 5 and their description of column 3, lines 39-62) a method of fabricating a high-density flat-cell mask ROM, including the steps of forming a pad-oxide (100) film and a nitride film (120) on a substrate (100), forming a mask pattern (125) on the nitride film (120), exposing the substrate by removing the nitride film and the pad oxide film (column 3, lines 63-66) and diffusing impurities to the exposed substrate (column 4, lines 50-55). Regarding the use of a mask pattern as blocking mask, this is a known practice in the semiconductor art in order to implant impurities on selected regions of a substrate.

Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the method as disclosed by Applicant's admitted prior art to include the claimed steps for forming the buried layers, as suggested by Wu, in order to provide a device with high-density and of smaller width (column 3, lines 39-48).

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

E.O
A.U. 2815
3/21/05

GEORGE ECKERT
PRIMARY EXAMINER